Pressure Contact Multi-Chip Packaging of SiC Schottky Diodes

Jose Ortiz Gonzalez, Olayiwola Alatise and Philip Mawby
School of Engineering
University of Warwick
Coventry, United Kingdom

Attahir M. Aliyu and Alberto Castellazzi
Power Electronics, Machines and Control Group
University of Nottingham,
Nottingham, United Kingdom

***Abstract*— Pressure contact packages have demonstrated an improved reliability for silicon devices due to the elimination of the weak elements of the packaging, namely wirebonds and solder. This packaging approach has not yet been widely studied for SiC devices, however, it is of high interest for applications like HVDC or rail traction, where the wide bandgap properties of SiC devices can be fully exploited and high reliability is critical. Current IGBT press-pack modules use Si PiN diodes for enabling reverse conduction, however, the use of SiC Schottky diodes would be beneficial given their better characteristics including low switching losses and lower zero temperature coefficient (ZTC) for electrothermal stability of diodes in parallel. A prototype for the evaluation of SiC Schottky diodes using pressure contacts has been designed, built and tested for both single die and multiple die.**

Keywords*— *Pressure contacts, Press-pack, Silicon carbide

I. INTRODUCTION

Pressure packaging is not a new packaging concept. It has already been used for large area thyristors and it is basically a semiconductor wafer compressed between two copper poles, using an intermediate contact to match the coefficient of thermal expansion (CTE) of the materials in direct contact [1].

Press-pack IGBTs are a suitable packaging alternative to the direct bonded copper (DBC) based power modules in applications which require an enhanced robustness and reliability. The improved reliability of press-pack assemblies arises from the elimination of the weak elements of the traditional DBC based power modules, namely the solder and wirebonds [1]. In the case of IGBTs, this packaging method has been used by different manufacturers, with different approaches to establish a good contact between the multiple semiconductor chips and the intermediate contacts for matching the CTE. From a global force applied to the module [2], to an individual spring for each chip [3], press-pack IGBT modules are commercially available now. These modules are mainly used in applications like HVDC and FACTS, which require a high reliability and robustness.

Silicon carbide appears as a suitable semiconductor for these applications, given its superior properties compared with silicon [4], nevertheless the lower power cycling capability demonstrated by silicon carbide devices and modules when the traditional packaging methods are used [5], is limiting the speed of adoption of SiC in these areas, which will fully exploit its wide bandgap properties. There are few studies of SiC devices in pressure packages and given the benefits of this packaging method a prototype for the evaluation of SiC using pressure contacts has been designed and evaluated.

The electrothermal characterization, power cycling results and studies on pressure imbalance between parallel chips using pressure contacts are presented in this paper.

II. PROTOTYPE FOR EVALUATION OF PRESSURE CONTACTS

A. Prototype design and single chip module characterization

A multiple chip prototype for the evaluation of SiC using pressure contacts is shown in Fig. 1. The chip selected for this module is a 1200 V/50 A SiC Schottky from Cree/Wolfspeed with datasheet reference CPW5-1200-Z050B. The intermediate contacts used for matching the CTE are made of molybdenum or aluminum graphite (ALG) [6], while the poles are made of copper with a 5 µm nickel plating.

The multiple chip prototype is an expansion of the single chip prototype which was used in [7, 8] for the evaluation of the impact of the intermediate contact material on the electrical and thermal characteristics in pressure contact assemblies. The intermediate contact materials evaluated were molybdenum and ALG.

The proposed prototype uses a global force applied to the module like the solution used in [2], which will be distributed between the different chips. In this pressure packaging system,

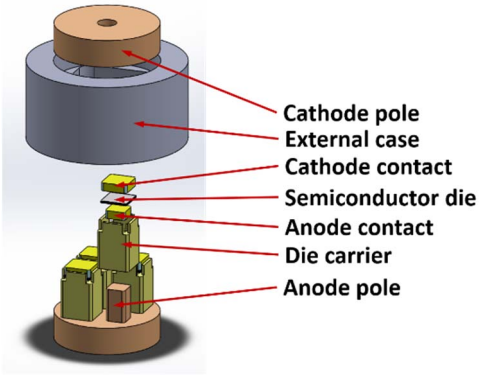

Fig. 1. Schematic of the multi-chip SiC Schottky diode using pressure contacts, where the different elements are identified.

This work was supported by UK Engineering and Physical Sciences Research Council (EPSRC) through the Underpinning Power Electronics Devices Theme (EP/L007010/1), Components Theme (EP/K034804/1) and Hub (EP/K035304/1).

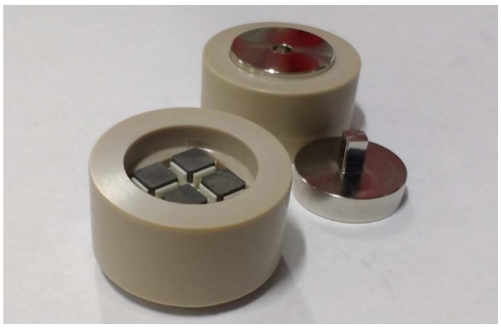

Fig. 2. Picture of the evaluated multiple and single chip SiC Schottky diode modules using pressure contacts in different assembly stages

the dimensional tolerances of the mechanical elements, as well as the thermal deformations would have an impact on the pressure distribution. A force of 10-20 N/mm2 is defined in [1] for an optimal electrical and thermal contact, hence in the case of multi-chip modules, the uneven pressure distribution could affect the electrical and thermal properties.

Using the single chip module, measurements for the evaluation of the impact of the clamping force have been done using the clamping system shown in Fig. 3. A box clamp model BX42 from GD Rectifiers [9], rated at different nominal clamping forces F for the nominal height of the module h, was used for applying the external force. The clamp is shown in Fig. 3(a) while the operating mechanism is shown in Fig. 3(b).

The on-state voltage (V_F), which is a function of the forward voltage of the diode V_{AK}, the contact resistances and resistivity of the materials, as shown in Fig. 4, has been measured for a series of currents and clamping forces for current pulse of 20 ms (t_{pulse}). The intermediate contacts used are made of molybdenum without any plating. Fig. 5(a) shows the calibration measurements for clamping forces F of 300 N and 500 N. As expected, increasing the clamping force reduces the on-state voltage through a reduction of the contact resistances. The average reduction of the forward voltage is 1.8 %.

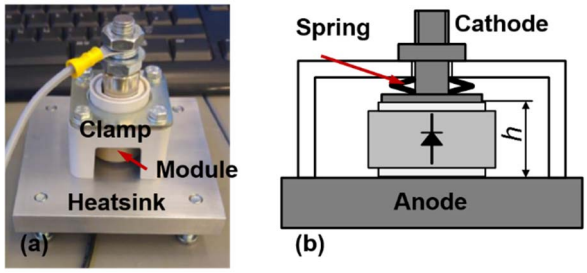

Fig. 3. Detail of the assembly of the clamp and the press-pack module. (a) Real prototype, (b) Operating mechanism of the clamp

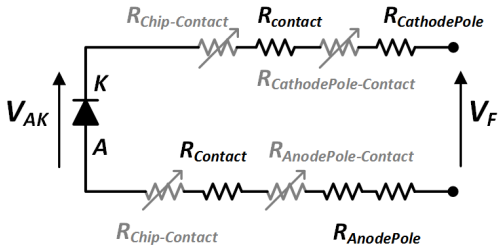

Fig. 4. Electrical schematic of the press-pack diode

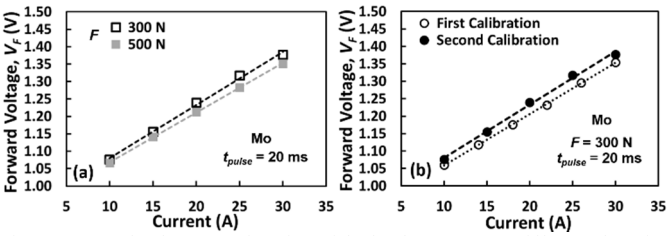

Fig. 5. Forward voltage as a function of the load current: (a) Different clamping forces (b) Same clamping force, different calibration measurements

A new characterization using the same rated clamp, hence the same nominal clamping force, has been done and the results are presented in Fig. 5 (b). Comparing the forward voltages for the same clamping force of 300 N, the average difference between the forward voltages between both calibrations is 2.2 %. It is important to mention that small clamping force variations can appear due to the tightening procedure.

The results presented in Figs. 5(a) and 5(b) show the importance of an uniform clamping force distribution in multi-chip modules and how a difference in the effective clamping force together with the inherent differences between the intermediate contacts and chips could have an impact on the electrothermal performance of the module, as the electrical and thermal resistances are affected by the clamping force through the electrical and thermal contact resistances respectively. It is important to mention that for a full study of the contact resistances, the plating, roughness and flatness of the materials in contact should be considered, as these properties affect the contact thermal and electrical resistances [10].

B. Multi-chip module characterization

The evaluation of the electrical characteristics of the multi-chip module has been done using clamps rated at 500 N and 2000 N. Assuming equal distribution of forces among the parallel chips, the effective clamping forces are 125 N/chip and 500 N/chip respectively. The forward voltage was captured for 15 s pulses at different DC currents and the results are presented in Fig. 6. From the results shown in Fig. 6, the forward voltage increases with increasing current and it is higher for the lower clamping force. The currents are below the ZTC, hence the decreasing voltage during the duration of the heating pulse.

The impact of the clamping force on the forward voltage is clearly observed in Fig. 7(a), where the forward voltages for the same current and clamping forces of 500 N and 2000 N are compared in the same graph. An initial steep change in the forward voltage is observed for the lower clamping force, indicating a faster temperature increase, more accused at the lower clamping force.

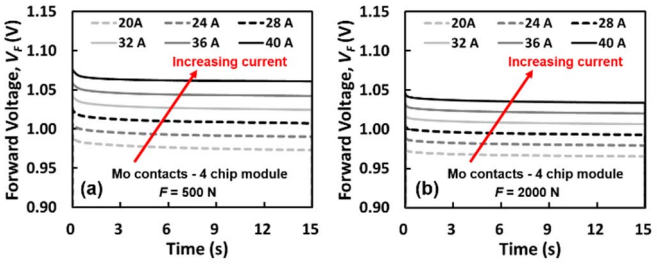

Fig. 6. Characterization of the forward voltage of the multi-chip module for different DC current pulses. (a) F= 500 N (b) F=2000 N

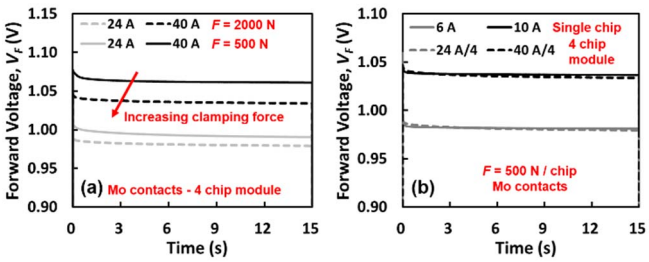

Fig. 7. (a) Impact of the clamping force on the forward voltage during a DC pulse for a multi-chip module, (b) Forward voltage during a DC pulse for single chip and multi-chip modules for an effective clamping force of 500 N

Fig. 7(b) compares the measured forward voltage for a single chip module and a clamping force of 500 N, with the measured forward voltage for a multi-chip module and a clamping force of 2000 N. A minimal difference between forward voltages can be observed, hence the effective individual clamping force can be identified as 500 N.

C. *Power cycling of single chip modules*

Power cycling is an effective tool for the evaluation of the degradation of the packaging when it is subjected to thermomechanical stresses during heating/cooling cycles. The characterization of the thermal impedance is usually a good indicator of damage to the packaging and valuable information can be obtained from these tests.

Studies of the power cycling of a single chip using ALG and molybdenum have been performed using advanced power cycling equipment which can characterize the thermal impedance during the tests [11]. Single chip modules were subjected to 19000 cycles of a 30 A heating current for 30 s with a cooling time of 30 s. The thermal impedance was characterized every 200 cycles and results are shown in Fig. 8, where the thermal resistance R_{TH} as a function of the number of cycles is shown for both intermediate contact materials. From the power cycling results, it can be observed that there is no overall increase in the thermal resistance during the tests and the thermal resistance is higher when molybdenum contacts are used.

The periodic variations on the thermal resistance are caused by periodic variation in the pressure at the interfaces during the power cycling, i.e. the expansion/contraction cycle of the die and intermediate contacts. This can lead to a non-uniform force distribution within the module, together with mechanical deformation of the assembly, as shown in Fig. 9.

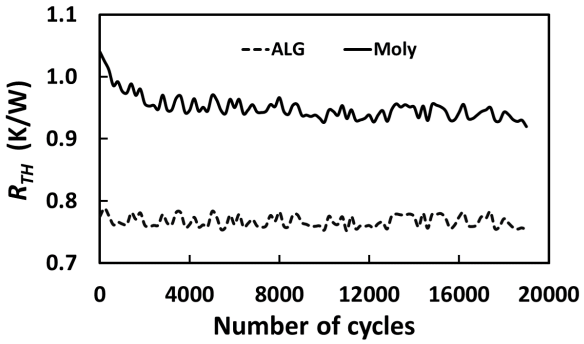

Fig. 8. Thermal resistance R_{TH} during power cycling of a single chip press-pack diode using ALG and molybdenum contacts

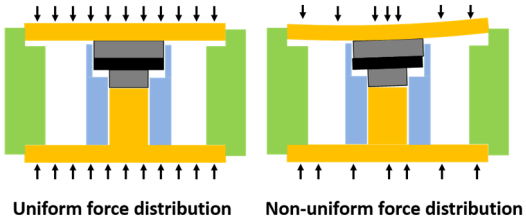

Fig. 9. Representation of the impact of the uniformity of the force distribution and mechanical deformation in a press-pack module assembly

In the case of multiple chip modules, this non-uniform force distribution can generate an increased contact resistance for some of the chips, which will cause current imbalance within the module, as well as differential thermal resistances between chips. This was identified as a failure mechanism in [12].

III. Impact of Clamping Force Imbalance In Multiple Chip Modules

In the previous measurements the clamp was properly adjusted and the force distribution between chips can be assumed balanced. However, as the power cycling results in the previous section show, the force distribution can have an impact on the performance of multiple chip press-pack modules. The reduced clamping force can be emulated if the bolts of the BX42 clamp are not uniformly tightened. Starting from a loose clamp, the forward voltages at different stages of the tightening procedure are shown in Fig. 10. It is clearly observed how the forward voltage is higher for a lower clamping force (i.e. loose clamp) while for a proper tightened clamp the forward voltage is low. The load current used for this test was 40 A, which in case of equal current sharing should be below the ZTC, hence the forward voltage should decrease during the self-heating of the diode.

It is clearly observed how the forward voltage is higher at low clamping forces due to the higher contact resistances. The forward voltage could be an indicator of uneven current sharing, with the higher voltage as an indicator of a global increase in the contact resistance. The change in the slope for the voltage during self-heating can also identify current imbalance between chips. In the case of the loose clamp, the forward voltage increases after an initial steep dip in the forward voltage, clearly an indicator of a clamping force imbalance between the paralleled chips.

The current sharing between parallel chips and the forward voltage could be health indicators for multi-chip press-pack

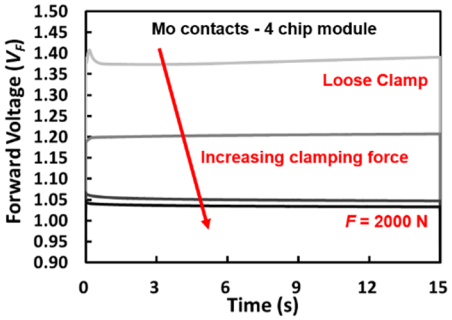

Fig. 10. Forward voltage of a multi-chip diode during a heating pulse at different stages of the assembly/tightening of the clamp.

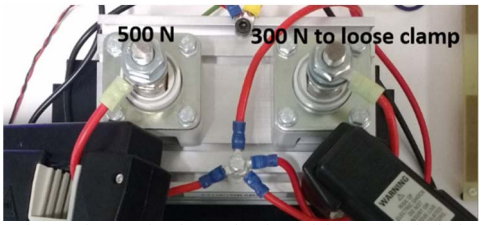

Fig. 11. Experimental setup for the evaluation of the current imbalance between parallel chips using pressure contacts

modules, hence the impact of the clamping force imbalance has been evaluated. Using the test setup shown in Fig. 11, where two single chip modules are connected in parallel using individual BX42 clamps, the non-uniformity of the clamping force can be studied. The clamps are rated at300 and 500 N respectively (low clamping force imbalance) and loosening one of the clamps a higher imbalance can be emulated.

The current level will also have an important role in the case of parallel connected devices. If the current is above the ZTC the hotter device will have a higher resistance, hence conducting less current. In the case of parallel devices using pressure contacts the device with a lower contact resistance will conduct more current, however in the case of SiC Schottky diodes, unipolar devices with a low ZTC, this initial current imbalance caused by the non-uniform clamping force will be electrothermally stable. Fig. 12 shows the measured diode currents I_D for two paralleled single chip modules and a load current I_{load}=40 A. Fig. 12(a) shows the case of a mild pressure imbalance (300-500N) where it can be observed how the current difference stabilizes due to the impact of the low ZTC.

Fig. 12(b) shows the measured currents for a case of extreme clamping force imbalance, where the 300 N clamp was loose. The initial current imbalance is caused by the different contact resistances, which cause the current to flow mainly through the properly clamped diode. However, as the operating point is above the ZTC, the currents converge because the hotter device is increasing its resistance. In the case of Si PiN diodes, bipolar devices with a higher ZTC, this could generate electrothermal instability, as the hotter device will take more current as its temperature increases. Measurements for a load current below the ZTC, namely 10 A, are shown in Fig. 13 (a). Given the low self-heating at this current level, the initial current imbalance stays as a stable imbalance, as the hotter device is not taking more current.

Fig. 13(b) shows the forward voltage captured for different clamping force imbalances and a load current of 40 A. It is clearly observed how the device conducting a higher current will determine the forward voltage. The initial negative slope in the

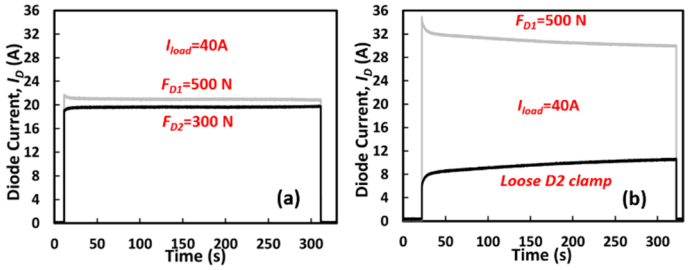

Fig. 12. Current sharing between parallel chips for a load current above the ZTC at (a) low clamping force imbalance, (b) high clamping force imbalance

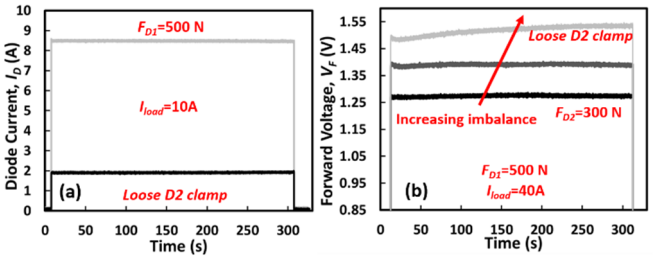

Fig. 13 (a) Current sharing between parallel chips for high clamping force imbalance and load current below the ZTC (b) Impact of the clamping force imbalance on the forward voltage for a load current above the ZTC

forward voltage could be used for identifying a clamping force imbalance between parallel chips. In the case of SiC Schottky diodes, if the current is above the ZTC, an initial negative slope indicates a reduction of current caused by the self-stabilization of the pressure imbalance.

IV. Conclusions

Press-pack modules can be a suitable packaging system for SiC Schottky diodes. Power cycling results show no degradation of the thermal impedance, however the mechanical clamping system has an impact on the thermal and electrical performance. Due to the continuous expansion/contraction of the elements within the module, differential clamping forces can appear between parallel chips.

In the case of multiple chip modules using pressure contacts, the current sharing between chips and the forward voltage, could be suitable health indicators.

References

[1] J. Lutz, H. Schlangenotto, U. Scheuermann and R. De Doncker, *Semiconductor power devices: Physics, characteristics, and reliability*. Springer Verlag, 2011.

[2] IXYS Press-Pack IGBT modules [Online]. Available: http://www.westcode.com/ppigbt.html

[3] ABB StakPak modules [Online]. Available: http://new.abb.com/semiconductors/stakpak

[4] J. Millán et al., "A survey of wide bandgap power semiconductor devices," IEEE Transactions on Power Electronics, vol. 29, no. 5, pp. 2155-2163, May 2014

[5] C. Herold et al., "Power cycling capability of Modules with SiC-Diodes," CIPS Conference 2014, Nuremberg, Germany, 2014, pp. 1-6.

[6] Schunk Hoffmann Carbon Technology AG, Aluminium Graphite composites brochure [Online]. Available: www.hoffmann.at

[7] J. Ortiz Gonzalez et al., "Development and characterisation of pressed packaging solutions for high-temperature high-reliability SiC power modules", Microelectronics Reliability, Volume 64, pp 434-439, September 2016

[8] J. Ortiz Gonzalez et al., "An initial consideration of silicon carbide devices in pressure-packages," IEEE ECCE Conference, Milwaukee, USA, pp. 1-7, September 2016

[9] GD Rectifiers Ltd. [Online], Available: http://www.gdrectifiers.co.uk/

[10] M. M. Yovanovich, "Four decades of research on thermal contact, gap, and joint resistance in microelectronics," in IEEE Transactions on Components and Packaging Technologies, vol. 28, no. 2, pp. 182-206, June 2005.

[11] Mentor Graphics T3ster [Online]
Available: https://www.mentor.com/products/mechanical/micred/t3ster/

[12] L. Tinschert et al., "Possible failure modes in Press-Pack IGBTs,", Microelectronics Reliability, Vol. 55, no. 6, pp. 903-911 May 2015